REMARKS

Applicants respectfully request entry of this Preliminary Amendment prior to the first Official Action and prior to calculating the fees for the application.

Applicants respectfully request consideration and allowance of claims 1-38.

The Director is authorized to charge any fee deficiency required by this paper or credit any overpayment to deposit account No. 23-1123.

Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor	: Judy L. Westby et al.	
Filed	: Herewith	Group Art Unit: ---
For	: METHOD AND APPARATUS TO REDUCE SERIAL COMMUNICATIONS PATH CONNECTION OVERHEAD	Examiner: ---
Docket No.:	S104.12-0060	

CLAIM STATUS AND SUPPORT

Express Mail No. EV178025422US
Date of Deposit: November 13, 2003

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

1. (Pending)A communications channel system for reducing arbitration overhead comprising:

a first channel node having a first port and a second port, each port supporting a fiber-channel arbitrated-loop serial communications channel, wherein each one of the ports arbitrates for control of that port's attached communications channel; and

an arbitration-and-control apparatus to reduce arbitrated-loop overhead, wherein the arbitration-and-control apparatus arbitrates for control of a loop of the communications channel and, after control is achieved, maintains control of the communications channel as long as at least a first predetermined amount of data is available within control of the channel node, wherein the first predetermined amount of data within control of the channel node includes at least some data not available for transfer to the communications channel.

2. (Pending) The system according to claim 1, further comprising:

a channel-node circuit chip, the chip having an on-chip data buffer, wherein the first predetermined amount of data includes a predetermined amount of on-chip data within the on-chip data buffer currently available for transfer to the communications channel; and

an off-chip memory, wherein the first predetermined amount of data further includes a predetermined amount of off-chip data, which is to be transferred to the communications channel but is currently not available for transfer, within the off-chip memory that is distinct from the predetermined amount of on-chip data.

3. (Pending) The system according to claim 2, wherein the predetermined amount of on-chip data includes a programmable amount of data.

4. (Pending) The system according to claim 2, wherein the predetermined amount of off-chip data includes a programmable amount of data.

5. (Pending) The system according to claim 2, wherein the predetermined amount of on-chip data includes a programmable amount of data, the predetermined amount of off-chip data includes a programmable amount of data, and the predetermined amount of off-chip data is a different amount than the predetermined amount of on-chip data.

6. (Pending) The system according to claim 5, further comprising:

a magnetic-disc-storage drive operatively coupled to the first channel node; and

a computer system having a second channel node, wherein the

second channel node is operatively coupled to the first channel node in a fiber-channel loop in order to transfer data between the first and second channel nodes through the fiber-channel arbitrated-loop serial communications channel.

7. (Pending)The system according to claim 1, further comprising:

a magnetic-disc-storage drive operatively coupled to the first channel node; and

a computer system having a second channel node, wherein the second channel node is operatively coupled to the first channel node in a fiber-channel loop in order to transfer data between the first and second channel nodes through the fiber-channel arbitrated-loop serial communications channel.

8. (Pending)The system according to claim 1, wherein the arbitration-and-control apparatus, for at least one transfer operation, delays the start of the transfer operation until after a second predetermined amount of data is available for transfer.

9. (Pending)The system according to claim 1, further comprising:

a channel-node circuit chip, the chip having an on-chip data buffer; and

an off-chip memory operatively coupled to supply data to the channel-node circuit chip, wherein the communications channel is an fiber channel arbitrated loop, and the loop is held open if at least one-half a frame of data is contained in on-chip data-frame buffer, and at least one frame of data are contained in off-chip memory.

10. (Pending)A disc drive comprising:

a rotatable disc;

a transducer in transducing relationship to the rotating disc;

a channel node having a first port and a second port, each port supporting a fiber-channel arbitrated-loop communications channel, each communications channel including a cyclic-redundancy code within data transmissions on the communications channel, the channel node operatively coupled to the transducer to communicate data; and

an arbitration-and-control apparatus operatively coupled to the channel node to reduce arbitrated-loop overhead, wherein the arbitration-and-control apparatus arbitrates for control of a loop of the communications channel and, after control is achieved, maintains control of the communications channel as long as at least a first predetermined amount of data is available within control of the channel node, wherein the first predetermined amount of data within control of the channel node includes at least some data not available for transfer to the communications channel.

11. (Pending) The disc drive according to claim 10, further comprising:

a channel-node circuit chip within the channel node, the chip having an on-chip data buffer, wherein the predetermined amount of data includes a predetermined amount of on-chip data within the on-chip data buffer currently available for transfer to the communications channel; and

an off-chip memory, wherein the predetermined amount of data further includes a predetermined amount of off-chip data, which is to be transferred to the communications channel but is currently not available for transfer, within the off-chip memory that is distinct from the predetermined amount of on-chip data.

12. (Pending)A communications method comprising steps of:

(a)(I) arbitrating for control of a loop of a fiber-channel arbitrated-loop serial communications channel; and

(b) maintaining control of the loop of the communications channel as long as a first predetermined minimum amount of data is available within control of the channel node, wherein the first predetermined amount of data within control of the channel node includes at least some data not currently available for transfer to the communications channel, whereby arbitrated-loop overhead is reduced.

13. (Pending)The method according to claim 12, wherein the maintaining step (b) further includes steps of:

(b)(I) determining an on-chip amount of data available in a channel-node circuit chip;

(b)(ii) determining an off-chip amount of data available in an off-chip memory; and

(b)(iii) comparing the on-chip amount of data available to a predetermined minimum-required amount of on-chip data;

(b)(iv) comparing the off-chip amount of data available to a predetermined minimum-required amount of off-chip data; and

(b)(v) maintaining control of the loop based on these comparisons.

14. (Pending)The method according to claim 13, wherein the maintaining step (b) further includes a step of:

(b)(vi) programmably changing the predetermined minimum-required amount of on-chip data and the predetermined minimum-required amount of off-chip data.

15. (Pending)The method according to claim 13, wherein the maintaining step (b) further includes a step of:

(b)(vii) programmably changing the predetermined minimum-required amount of off-chip data to a different amount than the predetermined minimum-required amount of on-chip data.

16. (Pending)The method according to claim 13, wherein the maintaining step (b) further includes a step of

(b)(viii) programmably changing the predetermined minimum-required amount of off-chip data.

17. (Pending)The method according to claim 12, further comprising a step of:

(c) transferring data through the fiber-channel arbitrated-loop serial-communications channel between a magnetic-disc-storage drive that is operatively coupled to the first channel node and a computer system having a second channel node, wherein the second channel node is operatively coupled to the first channel node by the fiber-channel arbitrated-loop serial-communications channel.

18. (Pending)The method according to claim 12, further comprising a step of

(d) beginning a transfer operation only after a second predetermined amount of data is available for transfer.

19. (Pending)A fiber-channel node controller system for reducing arbitration overhead comprising:

a first channel node having a first port and a second port, each port supporting a fiber-channel arbitrated-loop serial communications channel, each communications

channel including a cyclic-redundancy code within data transmissions on the communications channel; and

arbitration-and-control means for arbitrating for control of a loop of the communications channel and, after control is achieved, maintaining control of the communications channel as long as at least a first predetermined amount of data is available within control of the channel node, wherein the first predetermined amount of data within control of the channel node includes at least some data not available for transfer to the communications channel, thus reducing arbitrated-loop overhead.

20. (Added) A system for comprising:

a first serial device having n ports, each port supporting a serial communications path, wherein each one of the ports arbitrates for control of the serial communication path supported by that port; and

an arbitration-and-control apparatus configured to arbitrate for control of the serial communications path and, after control is achieved, maintain control of the communications path as long as at least a first predetermined amount of data is available within control of the first serial device, wherein the first predetermined amount of data within control of the first serial device includes at least some data not available for transfer to the serial communications path.

21. (Added) The system of claim 20 wherein n comprises one or more.

22. (Added) The system according to claim 20, further comprising:

a serial device circuit chip, the chip having an on-chip data buffer, wherein the first predetermined amount of data includes a predetermined amount of on-chip data within

the on-chip data buffer currently available for transfer to the serial communications path; and

an off-chip memory, wherein the first predetermined amount of data further includes a predetermined amount of off-chip data, which is to be transferred to the serial communications path but is currently not available for transfer, within the off-chip memory that is distinct from the predetermined amount of on-chip data.

23. (Added) The system according to claim 22, wherein the predetermined amount of on-chip data includes a programmable amount of data.

24. (Added) The system according to claim 22, wherein the predetermined amount of off-chip data includes a programmable amount of data.

25. (Added) The system according to claim 22, wherein the predetermined amount of on-chip data includes a programmable amount of data, the predetermined amount of off-chip data includes a programmable amount of data, and the predetermined amount of off-chip data is a different amount than the predetermined amount of on-chip data.

26.(Added) The system according to claim 25, further comprising:

a data storage device operatively coupled to the first serial device; and

a computer system having a second serial device, wherein the second serial device is operatively coupled to the first serial device in order to transfer data between the first and second serial device through the serial communications path.

27.(Added) The system according to claim 20, further comprising:

a data storage device operatively coupled to the first serial device; and

a computer system having a second serial device, wherein the second serial device is operatively coupled to the first serial device in order to transfer data between the first and second serial device through the serial communications path.

28. (Added) The system according to claim 20, wherein the arbitration-and-control apparatus, for at least one transfer operation, delays the start of the transfer operation until after a second predetermined amount of data is available for transfer.

29. (Added) The system according to claim 20, further comprising:

a serial device circuit chip, the chip having an on-chip data buffer; and

an off-chip memory operatively coupled to supply data to the serial device circuit chip, wherein the communications path is held open if at least one-half a packet of data is contained in on-chip data-packet buffer, and at least one packet of data are contained in off-chip memory.

30. (Added) A data storage device comprising:

a storage medium;

a serial device having n ports, each port supporting a serial communications path, each serial communications path including a data protection code within data transmissions on the serial communications path, the serial device operatively coupled to communicate data; and

an arbitration-and-control apparatus operatively coupled to

the serial device to reduce connection overhead, wherein the arbitration-and-control apparatus arbitrates for control of the serial communications path and, after control is achieved, maintains control of the serial communications path as long as at least a first predetermined amount of data is available within control of the serial device, wherein the first predetermined amount of data within control of the serial device includes at least some data not available for transfer to the serial communications path.

31. (Added) The data storage device according to claim 30, further comprising:

a serial device circuit chip within the serial device, the chip having an on-chip data buffer, wherein the predetermined amount of data includes a predetermined amount of on-chip data within the on-chip data buffer currently available for transfer to the serial communications path; and

an off-chip memory, wherein the predetermined amount of data further includes a predetermined amount of off-chip data, which is to be transferred to the serial communications path but is currently not available for transfer, within the off-chip memory that is distinct from the predetermined amount of on-chip data.

32. (Added) A method, comprising:

arbitrating for control of a serial communications path; and

maintaining control of the serial communications path as long as a first predetermined minimum amount of data is available within control of the a first serial device, wherein the first predetermined amount of data within control of the first serial device includes at least some

data not currently available for transfer to the serial communications path, whereby connection overhead is reduced.

33. (Added) The method according to claim 32, wherein the maintaining control further comprises:

determining an on-chip amount of data available in a serial device circuit chip;

determining an off-chip amount of data available in an off-chip memory;

comparing the on-chip amount of data available to a predetermined minimum-required amount of on-chip data;

comparing the off-chip amount of data available to a predetermined minimum-required amount of off-chip data; and

maintaining control of the serial communication based on the comparisons.

34. (Added) The method according to claim 33, wherein the maintaining controls of the serial communication path as long as a first predetermined minimum amount of data is available further comprises:

programmably changing the predetermined minimum-required amount of on-chip data and the predetermined minimum-required amount of off-chip data.

35. (Added) The method according to claim 33, wherein the maintaining controls of the serial communication path as long as a first predetermined minimum amount of data is available further comprises:

programmably changing the predetermined minimum-required amount of off-chip data to a different amount than the predetermined minimum-required amount of on-chip data.

36. (Added) The method according to claim 33, wherein the maintaining controls of the serial communication path as long as a first predetermined minimum amount of data is available further comprises:

programmably changing the predetermined minimum-required amount of off-chip data.

37. (Added) The method according to claim 32, further comprising:

transferring data through the serial-communications path between a data storage device that is operatively coupled to the first serial device and a computer system having a second serial device, wherein the second serial device is operatively coupled to the first serial device by the serial-communications path.

38.(Added) The method according to claim 32, further comprising:

beginning a transfer operation only after a second predetermined amount of data is available for transfer.

39. (Added) A system comprising:

a first serial device having n ports, each port supporting a serial communications path, each serial communications path including a data protection code within data transmissions on the serial communications path; and

arbitration-and-control means for arbitrating for control of the serial communications path and, after control is achieved, maintaining control of the serial communications path as long as at least a first predetermined amount of data is available within control of the serial device, wherein the first predetermined amount of data within control of the serial device

includes at least some data not available for transfer to the serial communications path, thus reducing connection overhead.

SUPPORT FOR ADDED CLAIMS

Claims 20 and 29 are supported by the specification at col. 30, line 64 - col. 31, line 31; col. 8 lines 25-29; original claims 1 and 10 and col. 2, lines 33-43 and 50.

Claim 21 is supported by col. 30 line 66.

Claims 22, 28 and 30 are supported by col. 4, line 66; col. 5 line 17; col. 5 lines 43-53; and col. 31 lines 6-11; and original claims 2 and 9.

Claims 23-25 are supported by col. 31 lines 11-17; col. 5, line 61; col. 6, line 25 and original claims 3-5.

Claim 26 is supported by col. 31, lines 17-26; col. 8, lines 34-45; col. 5, lines 27-42 and original claim 7.

Claim 27 is supported by original claim 8.

Claim 31 is supported by col. 31 lines 27-44; col. 6 lines 48-52 and original claim 12.

Claim 32 is supported by col. 31 lines 45-65; col. 5 line 61-col. 6, line 25; and original claim 13.

Claims 33-36 are supported by col. 31 lines 45-65; and original claims 14-17.

Claim 37 is supported by original claim 18.

Claim 38 is supported by col. 30 line 64; col. 31 line 6; and original claim 19.

Respectfully submitted,

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